Acoustic micro imaging of flip chip interconnects

Tom Adams

Using a flip chip configuration to interconnect a die with its substrate gives the device a smaller footprint (very desirable in multi-chip modules) and avoids the register and planarity problems one would face with lead bonding, such as TAB interconnects. The drawback is that flip chips have very small and very critical internal bonds which must be inspected to ensure the reliability of the device. Visual inspection methods, which are the most widely used methods for the inspection of interconnect quality, are not adequate for the evaluation of flip chip attach. The solder joints are located below the die and the bonds are often located throughout the face of the chip, not just at the perimeter of the die. This renders them uninspectable by visual techniques.

The bonds of the solder bump to both the die and the substrate interface can be imaged and inspected with C-mode scanning acoustic microscopy (C-SAM). In research conducted at Sonoscan [Bensenville, IL, USA], bonding at both of these levels, the integrity of the solder bump itself, and any accompanying epoxy underfill were imaged.

The C-SAM is a reflection-mode acoustic microscope. The instrument's ultrasonic scan head, scanning a rectangular area of the sample, alternately beams ultrasound into the sample and receives the returned (or reflected) echoes. The speed of very high frequency ultrasound through typical semiconductor materials – ranging from 3000 m/sec to 9000 m/sec – means that the round trip elapsed time is very short. The ultrasound is reflected from various internal material interfaces in the interior of the sample. A perfectly homogeneous sample – a flawless monolithic ceramic, for example – would return echoes only from the top and bottom surfaces because it has no internal interfaces.

Flip chips, however, have at least two internal interfaces, the top and bottom surfaces of the solder bumps. Because of the very small size of the bumps, high acoustic frequencies of 100 or 150 MHz are typically used to achieve high resolution. Flip chips can be imaged from either the top or bottom surface, depending largely on the substrate. When imaged from the top, the ultrasound must travel through the die before being reflected; the die is generally very transmissive and presents no barrier. Imaging from the bottom through the substrate is successful if the substrate itself does not have too many interfaces, and in

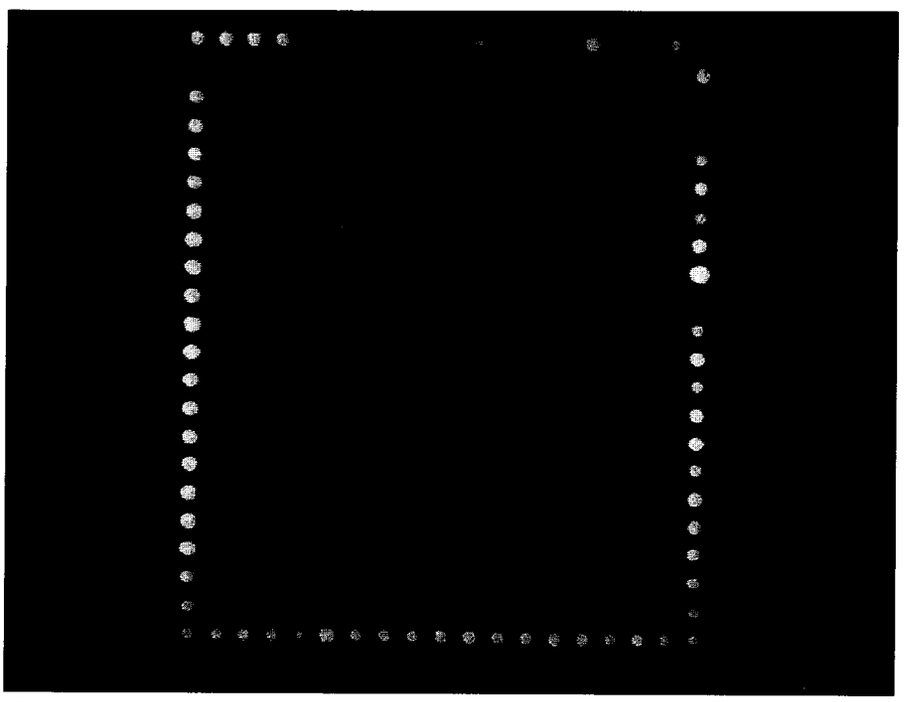

Figure 1. Imaged acoustically from bottom side through its silicon substrate, this device shows both missing and undersized solder bumps. The latter may pass electrical tests only to fail later. Note missing bonds (top) and variation in size of solder bonds. Minute bonds (top middle) may be electrically satisfactory now, but can be mechanically weak which means a shortened working life for the device. Note, no underfill is present in this sample.

particular if there are no interfaces with delaminations.

Return echoes from various internal levels within the flip chip arrive back at the scan head at slightly different times. These return echoes can be gated electronically in such a way that only those return echoes from a desired interface are used to produce an image; return echoes from above and below the desired interface are ignored and not imaged. Both the Z location and the depth of field of the gating can be selected, with the result that the ultrasound can be gated, for example, on the bump-chip interface, on the bump-substrate interface, or in the interior of the bump itself. Wider gating can be used to gate on both interfaces simultaneously; this technique may slightly degrade the image reflected from the more remote interface, but is useful in rapid screening of devices. In addition to gating, the focus of the ultrasound is optimized for the internal level which has been gated.

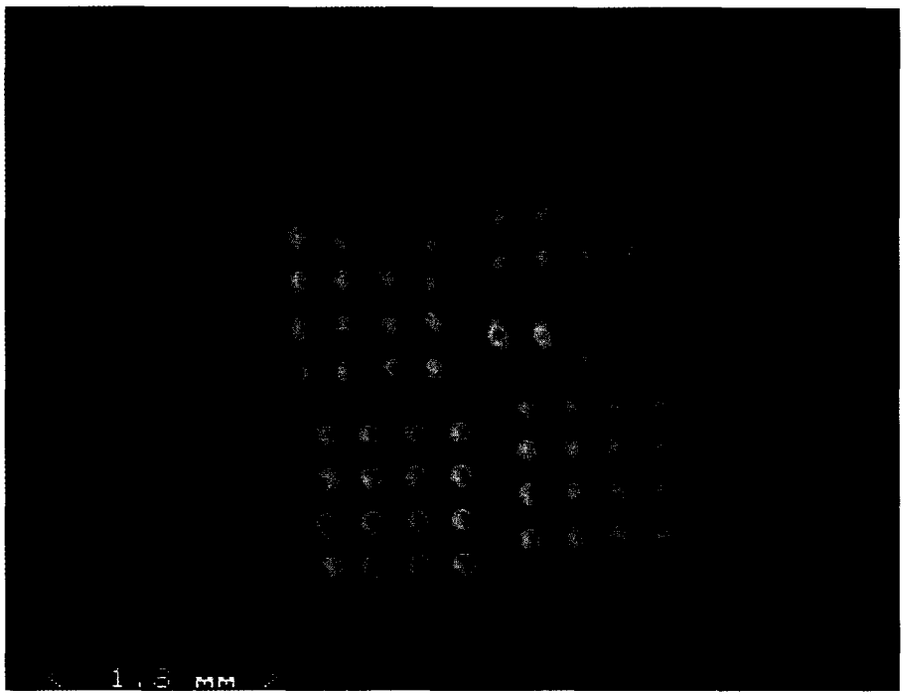

Figure 2. Misalignment chip to substrate, imaged through substrate of this chip caused some bumps to bridge, which would cause shorts. In addition, some bumps are missing. (No underfill).

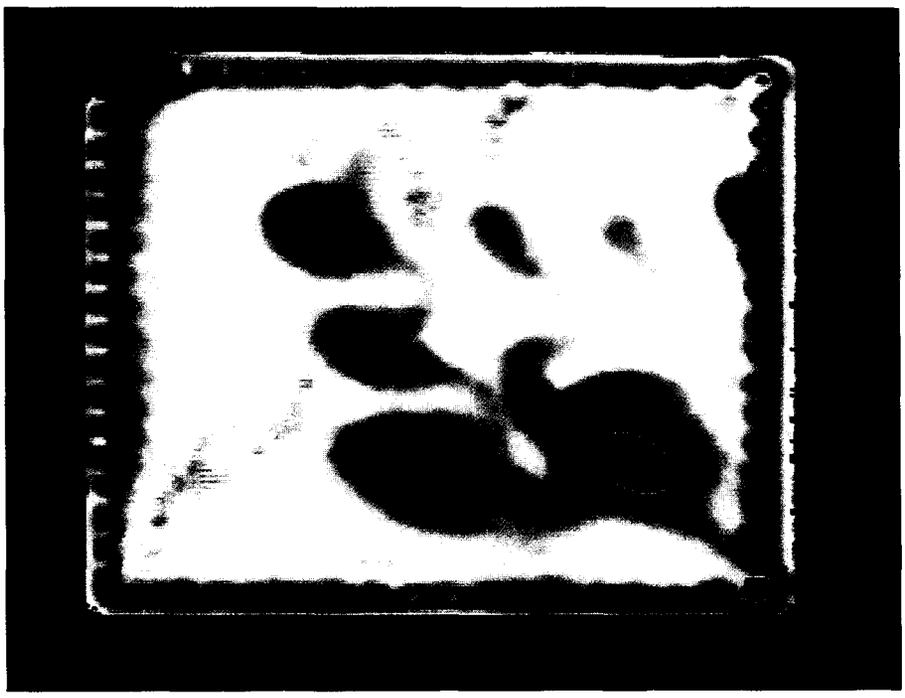

Figure 3. Flip chip with underfill. Imaged from top side through the die, this device shows that all solder bumps are intact, but that voids (e.g. top left corner etc in red) and irregular distribution of filler particles exist in the underfill.

The resulting acoustic image is made from two types of data: the amplitude of the returned echo; and the phase (polarity) of the returned echo. Both these attributes of the echo are governed by the acoustic impedance mismatch between the two materials at an interface. (The acoustic impedance of a material is defined as the density times the longitudinal velocity.) Dissimilar materials will show higher amplitude reflections at the boundary than materials with similar material properties. Polarity, registered by the Acoustic Impedance Polarity Detector (AIPD), is the shift upward or downward in acoustic impedance as the ultrasound crosses an interface. If the acoustic impedance increases, the polarity is positive; if the acoustic impedance decreases, the polarity is negative. Both amplitude and polarity data can be made visible in the displayed CRT image by various pseudocolour maps.

Imaging is not restricted to interfaces, however. It may be desirable to image the bulk of a material – i.e., the material between (but not including) two consecutive interfaces. In the present application, the material of greatest interest for bulk scanning is the solder bump itself. Interface scanning reveals the bonding of the solder bump to the die and to the substrate; bulk scanning reveals the internal characteristics of the solder bump. Just as the monolithic ceramic sample mentioned above would display no internal features if it were flawless, so the bulk scan of a defect-free solder bump will be without internal features. But a solder bump which contains a defect such as a void will display the image of the void.

Figure 1 is the acoustic image of a flip chip on a silicon substrate. Acoustic access to flip chips can be either from top or bottom; in this instance imaging was from the bottom through the substrate. Gating

was on the interface between the substrate and the solder bumps.

In this acoustic image, several solder bumps appear to be missing; but since gating is on the interface, the image actually shows only that the bond is missing. A few bonds are present, but appear very small acoustically. Small size indicates a small area of bonding to the silicon substrate. These bumps present a particular reliability problem because, while they may pass initial electrical tests, they are the bumps most likely to fail in use.

Figure 2 is the acoustic image of a different device, also imaged through the silicon substrate and gated at the substrate-bump interface. The skewed arrangement of the bumps results from misalignment of the bumps and the chip.

The misalignment is the likely cause of two further defects: some bonds are missing, and in two locations bumps have bridged with each other, a condition which causes connections to short out.

An epoxy underfill is sometimes used in flip chips to help secure the die to the substrate and alleviate the stress on the bumps. Figure 3 is the acoustic image of a device with epoxy underfill, imaged in this instance from the top side of the device through the die. The solder bumps running around the periphery of the chip are all present acoustically and all of equal size, indicating the absence of bump interface defects. There are defects, however, in the epoxy underfill.

Acoustic imaging of epoxy underfill in flip chips is much like the acoustic imaging of the epoxy packages which enclose integrated circuits: the main concerns are cracks, voids, and the distribution of filler particles within the epoxy. Both voids and uneven filler particle distribution can become the sites of thermal degradation, leading to cracks and the breaking of internal connections. In this image the underfill shows three voids, as well as much higher concentrations of filler particles in several regions.

Sonoscan, Inc.,
530 East Green Street,
Bensenville,
IL 60106 USA.
Tel: [1] 708 766-7088.
Fax: [1] 708 766-4603.

$200 M market for SiC components

A new study on silicon carbide (SiC) technology status and market applications has been released by Strategies Unlimited. Over the next decade electronic and optoelectronic devices based on SiC will enter the market in increasing volumes. The market for components based upon SiC is forecast to rise from $4 m in 1995 to $90 m by 2000 and to $200 m by 2005, representing a 48% p.a. CAGR.

Although SiC has been the subject of intensive research for the past two decades, the development of commercial components (with the exception of blue LEDs) has been slow to take place. However, recent technological progress has substantially increased the probability that SiC will achieve its potential in both electronic and optoelectronic components in the near future.

Exciting new developments in SiC technology are being achieved across a broad spectrum of applications. High-frequency power devices are being developed at Motorola for microwave and RF applications. General Electric is developing power and high temperature devices including sensors for jet engines. Westinghouse has fabricated very high-frequency MESFETs that perform at up to 26 GHz. In Sweden, ABB is working on high-power, high-voltage SiC rectifiers and other low-frequency power devices for industrial and utility use. Cree Research is shipping millions of SiC blue LEDs to markets around the world.

The report reviews the technology advances that have occurred in SiC crystal growth, epitaxial deposition, contact and interconnect formation, and packaging, which are the keys to unlocking the application of SiC components in commercial and military markets. It also identifies and discusses the driving forces for the implementation of SiC devices and the applications in which they are most likely to be used.

The principal electronic applications which show promise for SiC components are those requiring high-temperature, high-power and high-frequency operation. Device types include RF and microwave power devices, rectifiers, power switches, MESFETs, MOSFETs and JFETs. The principal optoelectronic applications for SiC are low-intensity blue LEDs and substrates for GaN-based high-intensity blue LEDs and blue laser diodes.

New high-temperature SiC devices are being developed for aircraft and automotive engine sensors, jet engine ignition systems, transmitters for deep well drilling, and a number of industrial process measurement and control systems. High-power SiC devices offer promise in solid-state lamp ballast, surge suppressors and power supplies. High-frequency power SiC devices are being developed for applications in high-frequency power supplies, cellular phone base stations, phased array radar systems, and small lightweight RF and microwave transmitters.

Small companies such as Cree Research and ATMI, as well as large companies such as Motorola, GE, Westinghouse and ABB are at the leading edge of SiC technology development. Government support ranges across a wide range of agencies, including ARPA, the US Air Force Wright Laboratory, the Office of Naval Research, and NASA Lewis Research Center, among others.

The comprehensive findings of this study are available in a 106-page report containing over 49 tables and figures. The major materials suppliers and component developers/suppliers are profiled, and a summary is provided of industrial, academic and government R&D activities in North America, Europe and Japan. A bibliography is attached with over 100 citations of recent work in the field.

The report, entitled *Silicon Carbide – 1995: Technology Status and Applications Analysis*, is available for immediate delivery. The price is $2,950.

■ *Contact: John Day, Strategies Unlimited, 201 San Antonio Circle, Suite 205, Mountain View, CA 94040. Tel/fax: (415) 941-3438/5120. email: strtultd@ix.netcom.com.*